D2

43. (Three Times Amended) A semiconductor capacitor comprising:

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one electrode surface comprises an electro-mechanically polished surface containing no hardening additive.

D3

48. (Twice Amended) A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished layer containing no hardening additive.

D4

49. (Amended) A semiconductor device comprising:

a substrate; and

at least one electro-mechanically polished metal layer consisting of a noble metal formed over said substrate.

50. (Amended) A semiconductor capacitor comprising:

a bottom electrode formed over a substrate;

an insulating layer formed over said bottom electrode; and

a top electrode formed over said insulating layer, wherein at least one electrode surface comprises an electro-mechanically polished metal surface consisting of a noble metal.

51. (Amended) A processor system comprising:

a processor; and

a memory device electrically coupled to said processor, said memory device comprising a substrate; and

a capacitor formed over said substrate, said capacitor comprising at least one electro-mechanically polished metal layer consisting of a noble metal provided over said substrate.